BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

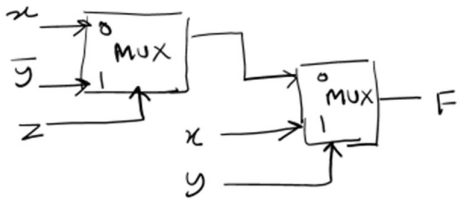
CLASS: MCA **SEMESTER : I**
BRANCH: MCA **SESSION : MO/2023**

SUBJECT: CA403 COMPUTER ORGANIZATION AND ARCHITECTURE

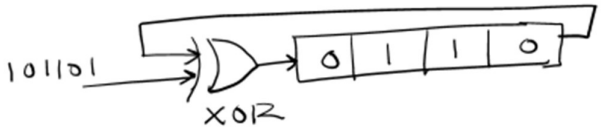
TIME: 3 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) (i) In the circuit below. Determine the output F.(2) CO2 ,K3 [5]



(ii)Determine the final value stored in the linear feedback shift register if the input is 101101 . (3) CO2,K3



Q.1(b) (i)A Machine has 26 bit architecture with one word long instruction. It has 64 registers each of which is 32 bits long. It needs to support 45 instructions which have an immediate operand in addition to two register operands. Calculate the maximum of the signed immediate operand. (2) CO1,K3 [5]
(ii)Give zero, one and two address instruction for the expression=B*M/(P+S)(3),CO2,K3

Q.2(a) Apply Booths algorithm to multiply -8X13, CO3,K3 [5]

Q.2(b) An instruction is stored at a location 200 with its address field at location 201.The address field has the value 400.A processor register R1 contains the number 400.Calculate the Effective address and the content of the Accumulator for the following addressing modes. (i) Register indirect(ii)autoincrement and autodecrement(iii)indirect and PC relative address,CO2,K5 [5]

Q.3(a) Consider a 3GHz processor with a three stage pipeline and stage latencies T1,T2 and T3 such that T1=3T2/5=2T3.If the longest pipeline stage is split into two pipeline stages of equal latency. Determine the new frequency ignoring the delays in the pipeline. CO4,K5 [5]

Q.3(b) Explain 1-bit and 2-bit branch prediction mechanism with an example. There is an instruction pipeline with four stages. The stage delays for each stage is 6 nsec, 7 nsec, 12 nsec, and 9 nsec respectively. Consider the delay of an inter-stage register in the pipeline is 1 nsec. Find the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation? CO4,K6,K3 [5]

Q.4(a) Explain with diagram parallel priority interrupt. CO5,K1 [5]

Q.4(b) Explain the causes of cache inconsistencies with neat diagrams. CO5,K2 [5]

PTO

Q.5(a) (i)In a two level hierarchy the top level has an access time of 20ns and the bottom level has an access time of 85ns.The hit rate on the top level is 90%.If the block size of cache is 8B.Calculate Effective memory access time.(ii) Consider a memory hierarch with a write back cache .The cache has an access time of 25ns,90% of all memory access are found in the cache itself .The main memory access time is 300ns.The 20% of the cache block are dirty .The cache block size is 4B.Determine the Effective memory access time.CO5,K4 [5]

Q.5(b) (i)A TLB access time is 50ns.Determine the Hit ratio for the TLB,if the Effective memory access time reduces from 400ns to 300ns.
(ii)What is the importance of DMAC ? The DMA module is transferring one 8 bit character in one CPU cycle from device to memory through cycle stealing at regular intervals. Consider a 4MHz processor. If 0.5% processor cycles are used for DMA, Determine the data transfer rate of the device in bits/secs.(2+1+2).CO5,K3,K2 [5]

:::::: 21/11/2023::::::E