BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: B.TECH **SEMESTER: VII**
BRANCH: ECE **SESSION: MO/2022**

SUBJECT: EC435 ASIC DESIGN

TIME: 2 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 25.
2. Candidates attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

				CO	BL
Q1	(a)	Give the brief history of VHDL.	[2]	CO1,CO2	L1
Q1	(b)	Explain the basic terminologies of VHDL with the help of examples.	[3]	CO1,CO2	L1
Q2	(a)	Write the VHDL code for a 4x1 MUX.	[2]	CO1,CO2	L3
Q2	(b)	Compare the three modelling styles in VHDL.	[3]	CO1,CO2	L4
Q3	(a)	How are sequential statements different from the concurrent statements?	[2]	CO1,CO2	L4
Q3	(b)	Explain the differences between the following: 1) signal and variable 2) sensitivity list and WAIT statement	[3]	CO1,CO2	L1
Q4	(a)	Compare FOR loop and WHILE loop.	[2]	CO1,CO2	L4
Q4	(b)	Discuss all the predefined data types in VHDL.	[3]	CO1,CO2	L1
Q5	(a)	Differentiate between array types and record types.	[2]	CO1,CO2	L2
Q5	(b)	Write VHDL code for half and full adder by making use of sequential statements.	[3]	CO1,CO2	L3

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