**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**
**(END SEMESTER EXAMINATION)**

**CLASS: B.TECH** **SEMESTER: VII**
**BRANCH: ECE** **SESSION: MO/2022**

**SUBJECT: EC435 ASIC DESIGN**

**TIME: 3 HOURS** **FULL MARKS: 50**

**INSTRUCTIONS:**
1. The total marks of the questions are 50.
2. Candidates attempt for all 50 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

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| Q1 | (a) | Explain the basic building blocks VHDL. | [2] | 1 | 2 |
| Q1 | (b) | Differentiate between concurrent signal assignment and sequential signal assignment. | [3] | 1 | 2 |
| Q1 | (c) | Write a VHDL code for Full adder using Half adder. | [5] | 2 | 3 |
| Q2 | (a) | Write the syntax of if and case statement and give example. | [2] | 1 | 2 |
| Q2 | (b) | Write the syntax of process statement and explain with the help of an example. | [3] | 1 | 2 |
| Q2 | (c) | Write the VHDL code for 8:3 encoder. | [5] | 2 | 3 |
| Q3 | (a) | Draw the date types diagram in VHDL. | [2] | 1 | 2 |
| Q3 | (b) | What are the different objects types of VHDL? | [3] | 1 | 2 |
| Q3 | (c) | Write VHDL code for half and full subtractor by making use of sequential statements. | [5] | 2 | 3 |
| Q4 | (a) | What are Deferred Constants? | [2] | 1 | 2 |
| Q4 | (b) | What is subprogram declaration? Explain with the help of example. | [3] | 1 | 2 |
| Q4 | (c) | Explain the asynchronous reset, asynchronous preset and clear with examples. | [5] | 1 | 2 |
| Q5 | (a) | Write a VHDL code for 2x1 MUX. | [2] | 2 | 3 |
| Q5 | (b) | Write a VHDL code for 4 bit Adder circuit. | [3] | 2 | 3 |
| Q5 | (c) | Write a VHDL code for Gray to Binary and Binary to Gray Converters | [5] | 2 | 3 |

**:::::21/11/2022 M:::::**