**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**
**(MID SEMESTER EXAMINATION)**

**CLASS: B.TECH** **SEMESTER: VII**
**BRANCH: ECE** **SESSION: MO/2022**

**SUBJECT: EC425R1 LOW POWER VLSI CIRCUITS**

**TIME: 2 HOURS** **FULL MARKS: 25**

**INSTRUCTIONS:**
1. The total marks of the questions are 25.
2. Candidates attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

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| Q1 | (a) | Define the phenomena " surface scattering " for short channel MOSFETs | [2] | CO1 |
| Q1 | (b) | Express the relation between W/L of a MOS with its trans conductance. Discuss the relation between $V_{GS}$, $V_{DS}$ and $V_T$ for off state, saturation and ohmic region of n-MOS transistor operation. | [3] | BL2 |
| Q2 | (a) | Why short -circuit power dissipation will arise in short channel MOSFETs? How can it be minimized? | [2] | CO1 |
| Q2 | (b) | Discuss about the leakage power dissipation and how can it be reduced? | [3] | BL2 |
| Q3 | (a) | What is transistor stacking effect? how it reduces the sub threshold leakage current? | [2] | CO2 |
| Q3 | (b) | In a complex CMOS logic gate circuit, if the number of internal circuits nodes are 15 and taking the assumption that node transition factor is 0.182, which is constant for all nodes. If the Vdd is 5 volt and the parasitic capacitance associated with each node is also same for all nodes is 0.012 uf with the clock frequency 100 Hz. Determine the total average power dissipation for the circuit. (Value of node voltage swing is also same for all is 3.5 volt, leakage current = 0.025u A, $V_T$ = 0.6 Volt, transistor amplification factor = 1). | [3] | BL3 |
| Q4 | (a) | How substrate bias reduces the static power dissipation? | [2] | CO2 |
| Q4 | (b) | "Voltage Islands" is one of the solution for dynamic power dissipation. Explain. | [3] | BL2 |
| Q5 | (a) | How weak inversion layer have been formed in short channel MOSFETs? | [2] | CO1 |
| Q5 | (b) | Explain technology mapping with the help of example and differentiate between rule based method and algorithm based method in context of technology mapping. | [3] | BL4 |

**:::::: 26/09/2022 ::::::M**