BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/2022**

SUBJECT: EC425R1 LOW POWER VLSI CIRCUITS

TIME: 3:00 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	What is the main difference between short channel MOSFET and long channel MOSFET?	[2]
Q.1(b)	Using Alfa power model, calculate the drain current of a short channel p-MOS if V_T = 0.3 V, V_{GS} = -3.7V, W/L=4, μ = 350cm^2 / Vs, ε = 3.9 *8.854 *10 $^{-12}$ F/N, t_{ox} = 100 Å and α = 1.3.	[3]
Q.1(c)	Why short circuit power dissipation will arise in short channel MOSFETs? Explain the reduction techniques ?	[5]
Q.2(a)	Substrate bias reduces the static power dissipation. How?	[2]
Q.2(b)	What is stacking effect? Explain with one example.	[3]
Q.2(c)	Discuss about the leakage power dissipation and how can it be minimized?	[5]
Q.3(a)	What is the basic difference between symmetric and asymmetric SRAM memory cell structure?	[2]
Q.3(b)	What is the meaning of technology node scale down ? what are its consequences upon dynamic power dissipation and static power dissipation of SRAM?	[3]
Q.3(c)	Explain the read function of 6T-SRAM with the help of circuit diagram.	[5]
Q.4(a)	Write down the conditions for reverse body biasing and forward body biasing .	[2]
Q.4(b)	How virtual power supply can be obtained for an SRAM? Write the advantages of virtual power supply for the SRAM circuit.	[3]
Q.4(c)	Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= ((A+B) C + D)'. You can assume both the original and complemented versions of each literal are available as gate inputs. Calculate the size of the n-MOS and p-MOS transistor connected in the logic function F.	[5]
Q.5(a)	How to design a p-channel active load for a CMOS inverter amplifier circuit? And what is its function in the circuit?	[2]
Q.5(b)	An OTA is a direct-coupled differential voltage-controlled current source. How? explain with circuit diagram.	[3]
Q.5(c)	Draw and explain the transfer characteristics curve of an active load CMOS inverter circuit with the help of circuit diagram. Drive the expressions for its voltage gain and frequency response.	[5]

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