**BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI**
**(END SEMESTER EXAMINATION)**

**CLASS: BTECH** **SEMESTER : VII**
**BRANCH: ECE** **SESSION : MO/2022**

**SUBJECT: EC413 REAL TIME EMBEDDED SYSTEM DESIGN**

**TIME: 3:00 Hours** **FULL MARKS: 50**

**INSTRUCTIONS:**
**1. The question paper contains 5 questions each of 10 marks and total 50 marks.**
**2. Attempt all questions.**
**3. The missing data, if any, may be assumed suitably.**
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
**5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.**

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| Q.1(a) | Define the Optical Display Interfacing. | [2] |
| Q.1(b) | Explain the Liquid Crystal Display Interfacing with suitable examples. Write the VHDL Code for Mux2:1. | [3] |
| Q.1(c) | Show the applications of Optical Sensor Interfacing. Write the Verilog @HDL code of 1bit adder. | [5] |
| Q.2(a) | Define the Sensors. | [2] |
| Q.2(b) | Explain the role of Signal Conditioning with Sensors. | [3] |
| Q.2(c) | Explain the role of Signal Conditioning with piezoresistive pressure sensors. Write the VHDL code for Decoder3:8. | [5] |
| Q.3(a) | Define the uses of Relay. | [2] |
| Q.3(b) | Show the basic diagram of Solenoid Valve and explain its characteristics. | [3] |
| Q.3(c) | Show the circuit diagram of BLDC motor and explain its functions. Write the Verilog@HDL code for Mux16:1 generic method. | [5] |
| Q.4(a) | Define the IoT (Internet of Things). | [2] |
| Q.4(b) | Explain the role of Internet of Things in Home Automation & Smart Education. | [3] |
| Q.4(c) | Show the interfacing between sensors with IoTs and RFID. Explain the requirement of security in IoT applications. Write the VHDL code for Decoder4:16 using vector method. | [5] |
| Q.5(a) | Define the Accelerometer. | [2] |
| Q.5(b) | Explain the Computers and Communication Networking with suitable examples. | [3] |
| Q.5(c) | Define the OSI model and explain the function of each layer in digital communications. Write the Verilog@HDL code for Up-down counter. | [5] |

**:::::23/11/2022:::::M**