BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI (END SEMESTER EXAMINATION)

CLASS: BTECH SEMESTER: V
BRANCH: ECE SESSION: MO/2022

SUBJECT: EC333 INTRODUCTION TO MICROCONTROLLERS

TIME: 3:00 Hours FULL MARKS: 50

INSTRUCTIONS:

- 1. The question paper contains 5 questions each of 10 marks and total 50 marks.
- 2. Attempt all questions.
- 3. The missing data, if any, may be assumed suitably.
- 4. Before attempting the question paper, be sure that you have got the correct question paper.
- 5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Apart from the accumulator in 8051, is there any register involved in multiply and division instruction [2] execution? Q.1(b) Why is the SP of MCS-51 an 8-bit and not a 16-bit register? [3] Write a program to generate a delay of 20msecs using 8051. [5] Q.1(c) Q.2(a) What is the difference between LCALL and ACALL instruction sets? [2] Q.2(b) When the MCU is powered on, the default register bank is bank 0. Write a program to switch to bank [3] 3 and then to switch to bank 1. Q.2(c) Draw the block diagram of the 8051 microcontrollers. Write the difference between the 8051 and 8031 [5] microcontrollers. Q.3(a) What is the difference between LJMP and SJMP instructions? [2] Q.3(b)What is meant by a register are bit addressable? [3] [5] Q.3(c)Why intel 8255 is designated as a programmable peripheral interface? How many timers are available in 8051? Distinguish between timer and counter. Q.4(a)[2] Explain the functions of the timer mode register (TMOD) and serial control register (SCON). [3] Write assembly language code to generate the square wave waveform at port 1.4 of 8051 Q.4(c) [5] microcontroller where ON time is 13 msec and OFF time 4 msec in a period using timer 1 in mode 1. The clock frequency is 12MHz. What is interfacing? Why is it essential to interface the keyboard and display devices to the 8051 [2] Q.5(a) microcontrollers? Illustrate with a suitable diagram the interfacing of the temperature sensor using port A of 8255 with Q.5(b) [3] memory-mapped schemes. Write short notes on a. Serial Communications b. Memory-mapped I/O and I/O mapped I/O [5] Q.5(c)

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