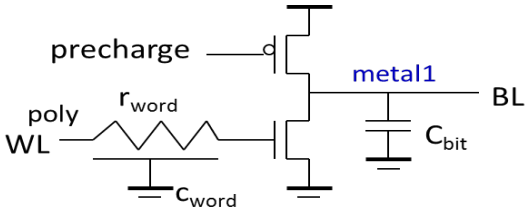
BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO/2022)

CLASS: BTECH **SEMESTER : V**
BRANCH: ECE **SESSION:MO-2022**
SUBJECT: EC325 R1DIGITAL SYSTEMS DESIGN WITH FPGAS
TIME: 03 Hours **FULL MARKS: 50**

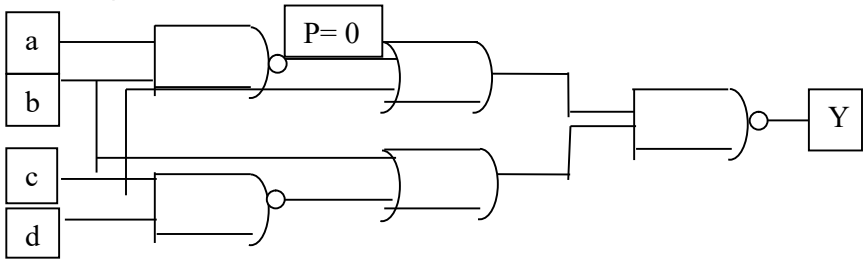
INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates

---

Q.1(a)	Why not incorporate programmable or adaptable components into all structures?	[2]
Q.1(b)	What are some of the most essential goals of the design's standard-cell placement and routing tools?	[3]
Q.1(c)	What are the different FPGA methodologies? Explain the same with neat diagram.	[5]
Q.2 (a)	Where do skew and jitter come from?	[2]
Q.2 (b)	Write a VHDL Code for 2 to 4 decoder using if else statement?	[3]
Q.2(c)	Design a XNOR gate with Verilog code using behavioral modeling?	[5]
Q.3 (a)	Mention a couple of the adder's optimization schemes?	[2]
Q.3 (b)	What are data paths in digital processor architectures?	[3]
Q.3(c)	Design a transmission gate adder circuit and explain its features.	[5]
Q.4(a)	Outline the several types of memory.	[2]
Q.4(b)	Implement and demonstrate the operation of the MOS cell's NOR ROM.	[3]
Q.4(c)	Evaluate the propagation delay associated with NOR ROM. Resistance/cell: 35ohm and 0.15ohm, wire capacitance/cell: 0.65 *f*F and 0.83 *f*F, and gate capacitance/cell: 5.10 *f*F and 2.60 *f*F, respectively for word and bit line.	[5]



Q.5(a)	Define the term d-frontiers and j-frontiers?	[2]
Q.5(b)	Determine the output Y for a stuck-at-fault at P=0.	[3]



Q.5(c)	Give the different classifications of open circuit faults and briefly explain them.	[5]

:::::: 29/11/2022 ::::::M