BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: B.TECH **SEMESTER: V**
BRANCH: ECE **SESSION: MO/2022**

SUBJECT: EC325 DIGITAL SYSTEM DESIGN WITH FPGAs

TIME: 2 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 25.
2. Candidates attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

				CO	BL
Q1	(a)	Identify few points of difference between semi-custom design and full custom design.	[2]	2	2
Q1	(b)	Distinguish difference between channeled and channel less array-based implementation approaches.	[3]	3	3
Q2	(a)	List the different types of macrocells. Give these types advantages.	[2]	2	1
Q2	(b)	Outline the standard-cell approach and give its advantages.	[3]	3	3
Q3	(a)	Differentiate between simulation and synthesis in brief.	[2]	2	2
Q3	(b)	Illustrate different data types offered in Verilog HDL? Discuss them with necessary syntax and an example.	[3]	3	3
Q4	(a)	Discus the classification of digital systems based on local clocks.	[2]	2	2
Q4	(b)	Identified three different techniques of field-programmable gate array (FPGA).	[3]	3	3
Q5	(a)	Explain about chew rate and jitter in digital system with suitable timing diagram.	[2]	2	2
Q5	(b)	List some design techniques for dealing with clock skew and jitter.	[3]	3	1

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