BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: B.TECH. **SEMESTER: V**
BRANCH: ECE **SESSION: MO/2022**

SUBJECT: EC319 VLSI SYSTEMS

TIME: 2 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 25.
2. Candidates attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data handbook/Graph paper etc. to be supplied to the candidates in the examination hall.

			Marks	CO	BL
Q1	(a)	Describe switching threshold (V_M) of a CMOS inverter. Explain how its value is obtained graphically. What is the desired value of V_M for a CMOS inverter in 0.25 µm process.	[2]	1	2
Q1	(b)	The data sheet of a CMOS inverter specifies the following parameters: V_{IHmin} =700 mV, V_{OHmin} = 900 mV, V_{ILmax} = 300 mV, V_{OLmax} = 100 mV. Calculate the HIGH-state noise margin (NM_H) and the LOW-state noise margin (NM_L).	[3]	1	3
Q2	(a)	Sketch gate to channel capacitance (CGC) as a function of degree of saturation and explain it.	[2]	1	3
Q2	(b)	Define propagation delays and rise and fall times. Substantiate your answer with suitable diagram.	[3]	1	1
Q3	(a)	Deduce the expression of energy E_{VDD}, taken from V_{DD} during the 0→1 transition of output node.	[2]	1	3
Q3	(b)	An inverter implemented in a generic 0.25 µm CMOS process has load capacitance C_L = 6 fF. Estimate the dynamic energy taken by it from the supply voltage.	[3]	2	3
Q4	(a)	Define pitch and crosstalk, which are related to interconnect. How many metal layers and poly layers are there in the generic 0.25 µm CMOS process?	[2]	2	1
Q4	(b)	The generic 0.25 µm CMOS process uses SiO_2 as dielectric material. In the same process if a 10 cm long, 1 µm wide and 1 µm thick aluminum wire is routed as first metal layer then compute the area (parallel plate) capacitance of interconnect. If the same process would use aerogel as dielectric material, what would have been the value of area (parallel plate) capacitance of interconnect of the same size	[3]	2	3
Q5	(a)	Schematize input pad with electrostatic discharge (ESD) circuit.	[2]	2	6
Q5	(b)	Explain purpose of each component and comment on the device length and oxide thickness of MOSFET used in that circuit.	[3]	2	4

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