BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

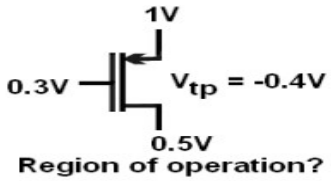
CLASS: BTECH **SEMESTER : V**
BRANCH: ECE **SESSION : MO/2022**

SUBJECT: EC319 VLSI SYSTEMS

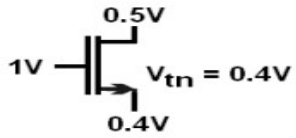
TIME: 3:00 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

				CO	BL
Q1	(a)	Find the region of operation of the pMOSFET and nMOSFET shown below.	[2]	1	2



Region of operation?

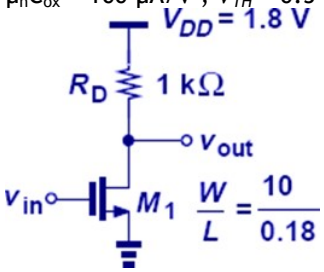


Region of operation?

Q1	(b)	List various secondary effects in a short-channel MOSFETs?	[3]	1	1
Q1	(c)	Write the expression of dynamic power consumption. Explain each term in it. Write the expression of Power-Delay Product (PDP) and Energy-Delay Product (EDP). Explain each term in them.	[5]	1	3
Q2	(a)	A wire, which is 10 cm long and 1 μm wide, is routed on the polycide, the sheet resistance of which is 4 Ohm-per-square. Compute the total resistance of the wire.	[2]	2	3
Q2	(b)	What is skin effect and skin depth? Express the equation of skin depth mentioning each term in minimum words.	[3]	2	2
Q2	(c)	Explain how a Schmitt trigger circuit can guard against noise-induced false switching when used in an input pad. Substantiate your answer with suitable diagram.	[5]	2	3
Q3	(a)	Explain why pseudo nMOS logic circuits are called ratioed circuits?	[2]	3	4
Q3	(b)	Diagram the transistor-level circuit diagram of an inverter and implement the same with Verilog HDL using switch-level modeling style.	[3]	3	4
Q3	(c)	Using CMOS logic styles realize the Co (carry out) function, which is given by Co= A.B+Ci.(A+B), and SUM function, which is given by SUM = A.B.Ci + (A+B+Ci), where Ci is the input carry.	[5]	3	4
Q4	(a)	Schematize transistor-level circuit of CMOS positive-level-sensitive D latch with minimum number MOSFET.	[2]	4	5
Q4	(b)	Schematize transistor-level implementation of SR flip-flop with NAND as well as NOR gate.	[3]	4	5
Q4	(c)	Schematize multiplexer-based NMOS latch using NMOS-only pass transistors. Explain its advantages and disadvantages with proper reasoning.	[5]	4	5

PTO

Q5	(a)	A MOSFET is biased at a drain current of 0.5 mA. If μ_n Cox = 100 μA/V^2, W/L = 10, and λ = 0.1V $^{-1}$, estimate its small-signal parameter g_m.	[2]	5	5
Q5	(b)	Estimate the small-signal voltage gain of the CS stage shown in Fig. 7.6 if I_D = 1 mA, $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5 V, and λ = 0. Verify that M_1 operates in saturation.	[3]	5	5



Q5	(c)	Schematize CS stage with load resistor R_D and source degeneration resistor R_S. Schematize its small signal model and derive the expression of its voltage gain.	[5]	5	6

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