BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO-2022)

CLASS: ALL **SEMESTER : V**
BRANCH: ECE **SESSION : MO/2022**

SUBJECT: EC303 MICROPROCESSOR & MICROCONTROLLER

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

Q.1(a) Write a small program to output the contents of Stack Pointer (SP) through two ports numbered 10 H and 20 H. [CO2, L3] [2]

Q.1(b) What is meant by hardware control matrix? Mention a suitable alternative for that. (Explain with block diagram) [CO1, L1] [3]

Q.1(c) A block containing equal number of even and odd bytes starts from location 'DATA'. The number of bytes (in BCD) in the block are given at location 'COUNT'. Write an 8085 based program to arrange them alternatively i.e., first odd, and next even. Store the result at location 'RESULT'. [CO2, L3] [5]

Q.2(a) Explain the following Instructions of 8085 µp with suitable examples [2]

i) DAA, ii) DAD RP, [CO2, L3]

Q.2(b) Differentiate between memory mapped I/O and I/O mapped I/O bringing out the relative merits and demerits. [CO2, L2] [3]

Q.2(c) Write down at least two purposes for which Read interrupt mask (RIM) instruction is used in 8085 µp. [5]

Write an 8085 based assembly language program to input 100 bytes of data serially through SID pin of 8085µp and store them in locations starting from DATA. Assume for each byte LS bit is arriving first, and the MS bit last. The bits are arriving at regular interval of time i.e., 1 millisecond between 2 bits and a delay subroutine 'ONEMIL' is available already. [CO2, L3]

Q.3(a) What do you understand by segmented memory? What are its advantages? How a particular location in a segment is accessed by the 8086 µp? [CO4, L2] [2]

Q.3(b) What do you understand by the pipelined architecture? How is it implemented in 8086? How do Request / Grant pins function in maximum mode of 8086µp? Which signals in minimum mode they replace? [CO4, L4] [3]

Q.3(c) What do you understand by even and odd addressing of memory in 8086 µp? Explain with the diagram, how is it achieved? Which addressing method is preferred and why? [CO4, L4] [5]

Q.4(a) Write down the different modes of operation of 8255 PPI. Where do we read the status in 8255 PPI? [CO3, L2] [2]

Q.4(b) Write an 8085 based program to generate a triangular wave of amplitude -2V to +2V. Use 8255 as the peripheral chip. [CO3, L5] [3]

Q.4(c) Write a program to generate a train of square wave having frequency 0.05 Hz using 8253 timer. Assume CLK0 frequency is 3 MHz, and PC_2 of 8255 is connected to GATE0 of 8253 timers. [CO3, L5] [5]

Q.5(a) Which port of 8051 µc does not have any alternate function and can solely be used for I/O? Explain the RESET Mechanism in 8051 µc and mention the default values of all the ports, PC, SP and PSW, following a reset. [CO4, L2] [2]

Q.5(b) Explain the addressing modes of 8051 µc with at least two examples for each mode. What is the limitation of indirect addressing mode? [CO4, L3] [3]

Q.5(c) Differentiate between General Purpose RAM (GPR) and Special Function RAM (SFR) of 8051 µc. Explain the Memory organization for the 128 bytes internal RAM of 8051 µc. [CO4, L3] [5]

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