BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER: III**
BRANCH: ECE+CS+IT+EEE **SESSION: MO/2022**

SUBJECT: EC203 DIGITAL SYSTEM DESIGN

TIME: 3 HOURS **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates.

				CO	BL
Q1	(a)	What is gray code and where it is used? How is it converted to Binary code?	[2]	1	1
Q1	(b)	Define each of the following electrical characteristics of logic gates: V_{OH}, V_{IL}, I_{OL}, $I_{IH.}$	[3]	1	2
Q1	(c)	Implement the logic function using CMOS, F=[(A+B)(C+D)(E+F(G+H))]'.	[5]	1	3
Q2	(a)	Define minterms and maxterms for three variables.	[2]	2	1
Q2	(b)	Simplify the following logic function using K-map. $F(A, B, C, D) = \sum (2, 7, 9, 14, 15) + \sum_d (0, 3, (10)$	[3]	2	2
Q2	(c)	Consider a 3-bit binary no. $X_3\ X_2\ X_1$ where X_1 is LSB. Design a circuit using NAND gate that will determine whenever the binary is greater than 3.	[5]	2	4
Q3	(a)	Give the logical design of 2x4 decoder.	[2]	3	1
Q3	(b)	Design the circuit of a BCD adder.	[3]	3	4
Q3	(c)	Implement the following expression using a single 8:1 multiplexer. $F(A, B, C, D) = \sum (0, 2, 3, 6, 8, 9, 12, 14)$	[5]	3	3
Q4	(a)	Draw the circuit of a serial-in-serial out shift register with J-K F/F.	[2]	4	1
Q4	(b)	Explain with diagram the working of a 3-bit ripple counter.	[3]	4	2
Q4	(c)	Design a synchronous counter with J-K F/F for state diagram: $1\rightarrow2\rightarrow3\rightarrow1$.	[5]	4	3
Q5	(a)	What is programmable logic device? What are the advantages of it? Name different types of it.	[2]	5	1
Q5	(b)	Explain the working of a PLA with a standard logic circuit and diagram.	[3]	5	2
Q5	(c)	Explain the working of a 4-bit synchronous up-down counter with diagram.	[5]	4	3

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