BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BTECH **SEMESTER : III**
BRANCH: CS/IT **SESSION : MO/2022**

SUBJECT: CS235 COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Explain the design principle of accumulator-based CPU. Also state the drawbacks of accumulator-based CPU.	[2]	1	2
Q.1(b)	Consider the following representation of a number in IEEE754 Single Precision floating point format with a bias of 127. S: 1 E: 10000001 F: 11110000000000000000000 Here S, E, F denote Sign , Exponent and Fraction components of the floating point representation. Find the decimal value corresponding to the above representation.	[3]	3	3
Q.1(c)	Using Booths multiplication algorithm show the multiplication of (-5)X(7)	[5]	3	5
Q.2(a)	Define addressing mode.	[2]	1	1
Q.2(b)	Write the zero, one, two and three address instruction for the following expression: X = (A-B)/(E+F)	[3]	2	5
Q.2(c)	Explain Direct and Indirect addressing mode with an example.	**[5]**	**2**	**5**
Q.3(a)	Differentiate between RISC and CISC.	[2]	3	3
Q.3(b)	Write the microoperations to be performed for an instruction MOV R_1, R_2.	[3]	3	5
Q.3(c)	Explain different pipeline hazards with their solutions.	[5]	4	5
Q.4(a)	What is the need to implement memory as a hierarchy?	[2]	5	4
Q.4(b)	Distinguish between SRAM and DRAM	[3]	5	3
Q.4(c)	What is meant by Cache Mapping? In how many ways mapping may be implemented? Explain Direct Cache Mapping technique with example.	[5]	1,3	1,5
Q.5(a)	Describe the various Bus Arbitration mechanisms.	[5]	5	5
Q.5(b)	Discuss Flynn's Taxanomy.	[5]	1	5

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