BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO/2022)

CLASS: B.TECH **SEMESTER : V/VII**
BRANCH: ECE/BT/CP&P/ME/PIE/EEE **SESSION : MO/2022**

SUBJECT: CS203 COMPUTER ORGANIZATION AND ARCHITECTURE
TIME: 03 Hours **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

Q.1(a) Represent $(1764)_{10}$ in binary coded decimal. [2]
Q.1(b) 1's complement of a negative octal number is 10111010. Find the number. [3]
Q.1(c) Represent $(0.00535)_{16}$ in single precision IEEE standard floating point format. [5]

Q.2(a) Explain Little Endian byte ordering [2]
Q.2(b) Write $(A+B*C)/(D^3+2)$ in 0-Addressing format [3]
Q.2(c) Summarize flynn's classification of computers [5]

Q.3(a) Describe virtual memory. [2]
Q.3(b) Demonstrate different cache mapping techniques. [3]
Q.3(c) Effective access time is 20% greater than the cache access time. Consider the cache access time and memory access time are 100ns and 500ns, respectively. Find the hit ratio. [5]

Q.4(a) Explain - Introducing dummy states may boost the minimum average latency [2]
Q.4(b) A non-pipeline processor has a clock frequency of 200 Mhz and has an average CPI of 4. Consider a 5 stage linear pipeline processor with clock rate of 150 Mhz. Compute the speed up for running 10,000 instructions. [3]
Q.4(c) [5]

	1	2	3	4	5	6	7	8
S1		X		X				
S2		X			X			
S3	X					X		X
S4			X				X	

Compute the minimum average latency from the above space time diagram.

Q.5(a) Demonstrate interrupt nesting or cycle stealing. [2]
Q.5(b) Explain different data transfer techniques in peripherals [3]
Q.5(c) Describe memory mapped and IO mapped interface or describe shared memory and message passing multiprocessors. [5]

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