BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION MO2022)

CLASS: MCA **SEMESTER : I**
BRANCH: MCA **SESSION : MO2022**

SUBJECT: CA403 COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 03 HOURS **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

Q.1(a)	Explain the differences between computer organization and architecture.	[2]	L2
Q.1(b)	Simplify the following Boolean function in product of sums form and draw the logic diagram with (i) OR-AND gates; (ii) NOR gates. $F(A, B, C, D) = \Sigma(2, 3, 4, 5, 6, 7, 11, 14, 15)$.	[3]	L4
Q.1(c)	Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2, or 3, the binary outputs is one greater than the input. When the binary inputs is 4, 5, 6, or 7, the binary output is one less than the input.	[5]	L6
Q.2(a)	Distinguish between Big-Endian and Little- Endian data storage schemes with suitable diagram?	[2]	L4
Q.2(b)	List out the characteristics of RISC and CISC style instruction sets with suitable example.	[3]	L1
Q.2(c)	Explain the different types of Addressing Modes with example.	[5]	L2
Q.3(a)	Define instruction cycle?	[2]	L1
Q.3(b)	Explain the hardwire and microprogramed control schemes with relevant diagram.	[3]	L2

Q.3(c)	Consider the pipeline with 5 stages: IF, ID, EX, M and W. Assume that each stage requires one clock cycle. Show how the following program segment for adding 2 arrays is processed and compare the clock cycles needed in non-pipeline system with pipelined system when result of the branch instruction i.e. content of is available after WB stage.
	LOAD R4 #400
	L1: LOAD R1, 0 (R4);
	LOAD R2, 400(R4);
	ADD R3, R1, R2;
	STORE R3, 0 (R4)
	SUB R4, R4, #4;
	BNEZ R4, L1;
		[5]	L6

Q.4(a)	Define Virtual memory?	[2]	L1
Q.4(b)	Differentiate between SRAM and DRAM with its typical cell structures.	[3]	L4
Q.4(c)	Explain the cache memory features, organization and its address mapping.	[5]	L2
Q.5(a)	Define multithreading?	[2]	L1
Q.5(b)	Distinguish between a subroutine and an interrupt-service routine?	[3]	L4
Q.5(c)	Explain cache coherence? How is cache coherence addressed in the multiprocessing system?	[5]	L2

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