BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE **SEMESTER: VII**
BRANCH: ECE **SESSION : MO/2019**

SUBJECT : MEC2067 VHDL & VERILOG

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) Give the brief history of VHDL. [2]
(b) Explain the basic terminologies of VHDL with the help of examples. [3]

Q2 (a) Discuss the different delay models in VHDL with examples. [2]
(b) Write the VHDL code for a 4x1 MUX. [3]

Q3 (a) How are sequential statements different from the concurrent statements? [2]
(b) Explain the differences between the following: [3]
1) signal and variable 2) sensitivity list and WAIT statement

Q4 (a) Explain different types of WAIT statements. [2]
(b) Compare FOR loop and WHILE loop. [3]

Q5 (a) Explain different object types in VHDL. [2]
(b) Write a note on composite types in VHDL. [3]

Q6 (a) Classify the user defined data types in VHDL. [2]
(b) Explain integer types and real types with examples. [3]

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