BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/19**

SUBJECT: MEC2067 VHDL & VERILOG

TIME:3:00 HOURS **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	Give the brief history of VHDL.	[2]
Q.1(b)	Explain the following w.r.t. VHDL (i) Driver (ii) Bus	[4]
Q.1(c)	Write the VHDL code for a Full adder using structural modeling.	[6]
Q.2(a)	What is sensitivity list in process statement?	[2]
Q.2(b)	Explain the syntax of For loop, While loop, If loop and Case statement.	[4]
Q.2(c)	Explain all the Wait statements along with examples.	[6]
Q.3(a)	Define various objects types in VHDL.	[2]
Q.3(b)	Explain various scalar types in VHDL with examples.	[4]
Q.3(c)	Write the VHDL code for 2-bit comparator.	[6]
Q.4(a)	What is the primary purpose of package?	[2]
Q.4(b)	What is subprogram declaration? Explain with the help of example.	[4]
Q.4(c)	Explain the asynchronous reset, asynchronous preset and clear with examples.	[6]
Q.5(a)	What is synthesis? Explain with diagram.	[2]
Q.5(b)	Explain logical, arithmetic, relational, shift operators.	[4]
Q.5(c)	Write a Verilog code for up-down counter with asynchronous preset and clear.	[6]
Q.6(a)	Explain how we can model the combinational and sequential logic in Verilog.	[2]
Q.6(b)	Draw the block diagram and model a Mealy FSM in Verilog.	[4]
Q.6(c)	Explain the blackjack model in Verilog.	[6]
Q.7(a)	What is resource allocation? Explain.	[2]
Q.7(b)	Describe the Dead code elimination and constant folding with examples.	[4]
Q.7(c)	Explain test bench. Write a test bench for a full adder.	[6]

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