BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : VII**
BRANCH: ECE **SESSION : MO/19**

SUBJECT: MEC1019 MICROELECTRONIC DEVICES AND CIRCUITS

TIME: 3.00Hrs. **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	Explain HOT carrier effect in short channel devices.	[2]
Q.1(b)	Draw the complete high frequency small signal equivalent circuit model and discuss the component used in equivalent circuit.	[4]
Q.1(c)	Discuss the accumulation, Depletion and inversion region for a MOS system under external bias with the cross-sectional view and energy band diagram.	[6]
Q.2(a)	Why we model physical faults as logical ones?	[2]
Q.2(b)	Describe the Built-In Self-Test (BIST) of fault modeling. Discuss its mode of operations.	[4]
Q.2(c)	What are the advantages of transistor level fault modelling? Discuss stack on and Stack off fault. Why transistor level fault detection is more difficult than gate level?	[6]
Q.3(a)	Discuss Bi-CMOS inverter circuit.	[2]
Q.3(b)	Why power dissipation is a major design consideration in mixed circuit design? What are the main sources of leakage currents?	[4]
Q.3(c)	What are the two configurations of cascade gain stage? Obtain the expression of total impedance at output node and overall gain for cascade gain stage.	[6]
Q.4(a)	Show Differential Pass Transistor Logic for AND/NAND and XOR/XNOR and show their Logical Explanation.	[2]
Q.4(b)	Discuss Progressive Transistor Sizing and input reordering for CMOS circuit.	[4]
Q.4(c)	What is the Non-inverting Property of Domino Logic? Discuss the methods to deal with Non-inverting Property of Domino Logic.	[6]
Q.5(a)	Draw the circuit diagram of Gilbert multiplier cell for four-quadrant multiplication.	[2]
Q.5(b)	Draw the circuit diagram of Gilbert multiplier cell for four-quadrant multiplication. What are the three different application of Gilbert Multiplier and how it depends on input values?	[4]
Q.5(c)	Why in differential pair the output CM level does not depend on change in input CM level? Derive the expression for small signal differential voltage gain.	[6]
Q.6(a)	Describe the Slicing floorplan representation.	[2]
Q.6(b)	Describe the goal of statistical modelling. Discuss the Epidemiological Concepts of device modelling.	[4]
Q.6(c)	What is the matching of device concept of layout? What are the rules for optimum matching? Discuss any four matching layout concepts with examples.	[6]
Q.7(a)	Discuss any one device modelling tool and its feature.	[2]
Q.7(b)	What is SPICE? Why SPICE's are used? How does SPICE work?	[4]
Q.7(c)	Describe the SPICE Element statement of BJT and FET in terms of Model, Statement and Parameter with an example.	[6]

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