BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: B.TECH **SEMESTER: III**
BRANCH: CSE/EEE/IT/ECE **SESSION : MO/2019**

SUBJECT : EC203 DIGITAL SYSTEM DESIGN

TIME: 2:00 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 25.
2. Candidates may attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.

Q1 (a) Distinguish between. [2]
(i) entity and architecture.
(ii) structural modeling and behavioural modeling in VHDL code.

Q1 (b) Perform the arithmetic operation (+17) + (-28) using [3]
(i) sign magnitude method,
(ii) sign 1's complement method and
(iii) sign 2's complement method.

Q2 (a) Explain the purpose of totem pole output stage of a 3-input TTL NAND gate with totem pole output driver. [2]

Q2 (b) List the advantages of CMOS logic. Design a CMOS logic circuit for the following Boolean function: [3]
$F = \sum_m(0,1,2,3,4)$

Q3 (a) Distinguish between Associative property and Distributive property of Boolean Algebra. [2]
Convert the following Boolean function to a minimum number of literals:
$$\boldsymbol{Y = [A\overline{B}\,(C + BD) + \overline{A}\overline{B}]C}$$

Q3 (b) Devise a combinational circuit for the following Boolean function [3]
$\boldsymbol{F = \overline{Y}\overline{Z} + \overline{X}\,\overline{Y} + \overline{W}XZ + WX\overline{Z}}$)
using NAND gates only.

Q4 (a) Formulate the Boolean function $\boldsymbol{F = \overline{A}\overline{C} + B}$ into a Canonical POS form. [2]

Q4 (b) Evaluate the simplification of the following Boolean function and obtain the minimal-SOP expression by Karnaugh map: [3]
$$\boldsymbol{F = \sum(1,2,5,6,7,9,15) + \sum_d(0,8,10,13)}$$

Q5 (a) Write the truth table of a full subtractor and construct it using a decoder and logic gates. [2]

Q5 (b) Perform the BCD-addition of 29 with 17. Construct the logic circuit for this BCD addition using 4-bit binary adders and logic gates. [3]

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