BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: M.TECH **SEMESTER : III**
BRANCH: CSE **SESSION : MO/19**

SUBJECT: CS605 HIGH PERFORMANCE COMPUTER ARCHITECTURE

TIME: 3 HOURS **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Write an explanatory note on Flynn's Architecture Classification. [5]

Q.1(b) Consider the following instructions: [5]

LOAD R1, A
ADD R2, R1
MUL R1, R3

R1, R2, R3: general purpose registers, and the first parameter in a computational instruction is both the source & destination.
Infer the various dependencies present amongst the instructions given above.

Q.2(a) Write an explanatory note on Crossbar Network. [5]

Q.2(b) Write an explanatory note on Scalability Metrics with respect to matching between computer architecture and application algorithms. [5]

Q.3(a) Compare RISC processors with CISC processors with respect to the following parameters: [5]
Instruction set size
Instruction formats
Addressing modes
General purpose registers
Cache design
Cycles per instruction (CPI)
CPU control.

Q.3(b) Consider a cache (M1) and RAM (M2) forming a two-level memory hierarchy with the following characteristics: [5]
M1: 64K 32-bit words, 5 ns access time
M2: 4M 32-bit memory words, 40 ns access time

Assume 8-word cache blocks with fully-associative mapping.
Show the mapping between M1 & M2.
Find the effective memory access time with a cache hit ratio= 0.95 & RAM hit ratio= 1.0

Q.4(a) Prove that the asymptotic speedup of a k-stage linear pipelined processor is at most k-times that of a k-stage linear non-pipelined processor. [5]

Q.4(b) Explain the cache coherence problem due to: [5]
data sharing
process migration

Q.5(a) Write an explanatory note on vector instruction types. [5]

Q.5(b) Discuss context-switching policies and processor efficiencies in the domain of multi-threaded architectures. [5]

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