BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: MCA **SEMESTER : I**
BRANCH: MCA **SESSION : MO/19**

SUBJECT: CA403 COMPUTER ORGANIZATION AND ARCHITECTURE

TIME:3:00 HOURS **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) (i) Simplify the Boolean expression using the minimal term A(A + B) + (B + AA)(A + B). [5]
(ii) Apply DeMorgan's Theorem to simplify ((A+D)'. (B'+C)')'

Q.1(b) Convert the decimal numbers -12 and 9 to 5-bit 2's-complement numbers, then perform addition and subtraction on each pair. Indicate whether overflow occurs or not. [5]

Q.2(a) In a RISC processors instruction set, the Immediate and Absolute modes restrict the operand size to 16 bits. Discuss how can a 32-bit value that represents a constant or a memory address be loaded into a processor register. [5]

Q.2(b) Registers R4 and R5 contain the decimal numbers 2000 and 3000 before each of the following addressing modes is used to access a memory operand. Compute the effective address (EA) in each case? (a) 12(R4) (b) (R4,R5) (c) 28(R4,R5) (d) (R4) + (e) − (R4) [5]

Q.3(a) Explain the working of control unit in the computer system and also explain the difference between Hardwired control unit over Micro-programmed control unit. [5]

Q.3(b) Analyze the effect of increasing the number of stages in a pipeline on its throughput. Also discuss how is the instruction throughput calculated. [5]

Q.4(a) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. [5]
(i) Calculate the number of bits required for addressing the main memory.
(ii) Calculate the number of bits needed to represent the TAG, SET and WORD fields.

Q.4(b) Explain the difference between (i) Logical address and physical address (ii) Page table and segment table [5]

Q.5(a) When a device interrupt occurs, how does the processor determine which device issued the interrupt? [5]

Q.5(b) (i) Consider a program whose execution time on some computer is *T*. As a performance enhancer, parallel processing is introduced. Assume that a fraction *f* of the execution time is affected by this enhancement. If *p* is the factor by which the portion of the time is reduced due to performance enhancement, what will be the new execution time? [5]
(ii) Explain in brief the working of a system that is capable of processing multiple data elements in parallel using a single instruction.

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