BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE **SEMESTER: VII/ADD**
BRANCH: ECE **SESSION : MO/2018**

SUBJECT : MEC1019 MICROELECTRONIC DEVICES AND CIRCUITS

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) Briefly explain channel length modulation and threshold lowering due to body effect with proper diagrams. Write corresponding modified expression. [2]

(b) Derive the small signal model (g_m, g_{gs}, r_0, C_{sb}, C_{db}) for an NMOS transistor with I_D = 100 µA. V_{SB} = 1 V, V_{DS} = 2V. Device parameters are ϕ_f = 0.3 V, W= 10 µm, L= 1 µm, γ= 0.5 $V^{1/2}$, k' = 200 µA/V^2, λ= 0.02 V^{-1}, t_{ox} = 100 angstroms, ϕ_0 = 0.6 V, C_{sb0}= C_{db0} = 10 fF. Overlap capacitance from gate to source and gate to drain is 1 fF. Assume C_{gb} = 5fF, $C_{ox=}$ 3.45 fF/ µm^2. [3]

Q2 (a) Draw a circuit diagram of a CMOS inverter. Draw its transfer characteristics and explain its operation. Obtain the expression of V_{1L} Resistive load MOS inverter [2]

(b) Arrange the following terms Coating, Patterning, Etching, Exposing, Developing, Masking in proper order and discuss each process with neat and clean diagram. [3]

Q3 (a) Show how the resistance, capacitance and delay are affected due to scaling of short wire interconnects. With appropriate diagrams? [2]

(b) What is fault detectability? Define observability and controllability. Discuss fault masking with one example. [3]

Q4 (a) Define Fault Equivalence Classes, Equivalence fault collapsing and fault dominance. How equivalence fault collapsing and fault dominance help in reduction of the set of faults to be analysed? [2]

(b) What is the aim of Scan design strategy for testing? Discuss the normal scan design test procedure. What are the disadvantages of normal scan design strategy? [3]

Q5 (a) Draw the current follower current mirror circuit. Derive the expression of r_{out} for a current follower current mirror. what is the main drawback of this circuit. [2]

(b) Assume all Transistor have W/L = 100 µm/1.6 µmin common source Amplifier and µn Cox = 90 µm/V2, µp Cox = 30 µm/V2, Ibias = 100 µm, rds-n (Ω) = 800 L (µm) /I_D (mA) and rds-np(Ω) = 1200 L (µm) /I_D (mA). What is the gain of the stage? [3]

Q6 Write short note on any two of the following [5]
- (a) Casecade Current Mirror
- (b) Wilson Current Mirror
- (c) Super MOS transistor

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