BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : VII/ADD**
BRANCH: ECE **SESSION : MO/18**

SUBJECT: MEC1019 MICROELECTRONIC DEVICES AND CIRCUITS

TIME: 3:00 HRS. **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a)	Discuss the required properties of a mixture or chemical used for wafer cleaning?	[2]
Q.1(b)	Obtain the expression of V_{IH} and V_{IL} of resistive load MOS inverter.	[4]
Q.1(c)	Discuss n well fabrication process of CMOS inverter with proper diagrams?	[6]
Q.2(a)	What is Ad-hoc Method of fault modeling? What is its limitation?	[2]
Q.2(b)	What is repeatability and Survivability in fault modeling?	[4]
Q.2(c)	What is short circuit and open circuit fault? Discuss with one example. How it can be rectify?	[6]
Q.3(a)	How the RC delay is affected by scaling?	[2]
Q.3(b)	What is gain boosting? Discuss one gain Boosting technique?	[4]
Q.3(c)	For a differential gain stage with p mos current mirror biasing and n mos input transistors, calculate rout and Av.	[6]
Q.4(a)	Draw cross sectional view of a BiCMOS inverter circuit.	[2]
Q.4(b)	What is the non-inverting limitation of domino logic gate? Explain one method to deal with the Non-inverting Property of Domino Logic.	[4]
Q.4(c)	Outline the main features of Dynamic gate. Discuss charge leakage and charge shearing issues in dynamic gates.	[6]
Q.5(a)	Draw the circuit diagram of Gilbert multiplier cell for four-quadrant multiplication.	[2]
Q.5(b)	Explain the working of active loaded MOS Differential pair.	[4]
Q.5(c)	Derive the expression for common mode gain of the MOS differential.	[6]
Q.6(a)	Describe the goal of statistical modeling.	[2]
Q.6(b)	Describe the absolute chip floorplan representation and differentiate it with Slicing floorplan representation.	[4]
Q.6(c)	List any three statistical simulation techniques are used to analyze circuits. What would be the best source of statistical data for generating statistical models?	[6]
Q.7(a)	What is the model of a device? Differentiate between Device modeling and Circuit simulation.	[2]
Q.7(b)	What are the different types of Analog Circuit simulation? How does circuit simulator work?	[4]
Q.7(c)	Describe the SPICE Element statement of Diode and BJT in terms of Model, Statement and Parameter with an example.	[6]

:::::10/12/2018:::::M