BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE **SEMESTER : V**
BRANCH: ECE **SESSION : MO/18**

SUBJECT: EC5205 DATA COMMUNICATION

TIME: 3.00 HOURS **FULL MARKS: 60**

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) What is meant by Attenuation Distortion? How is it caused? How can it be minimized? [2]

Q.1(b) If the received signal level for a digital system is -151dBW and the receiver system effective noise temperature is 1500 K, what is the E_b/N_0 for a link transmitting at a rate of 2400 bps? [4]

Q.1(c) Compare the differences between Hierarchical and Layered approaches in Computer Communication Architecture. [6]

Q.2(a) What is meant by a Self-clocking code? Give an example of such a code. What is its advantage in Synchronous transmission? [2]

Q.2(b) Where do you apply Scrambling techniques? What are their design goals? Briefly explain any one example of Scrambling techniques. [4]

Q.2(c) What is meant by Companding? What is meant by the dynamic range of input signal power? Explain with the help of a diagram, how Companding improves the dynamic range of input signal power. [6]

Q.3(a) Differentiate between Asynchronous transmission and Synchronous transmission, mentioning the relative merits and demerits of both techniques. [2]

Q.3(b) Show how you will interconnect two DTEs which are near to each other for intercommunication using EIA-232 standard. Justify all interconnections. [4]

Q.3(c) Compute the frame to be transmitted in a CRC scheme, for a Message 1011010111001 if the Generator Polynomial is $x5 + x^3 + x + 1$. [6]

Q.4(a) Differentiate between Normal Response Mode (NRM) and Asynchronous Response Mode (ARM). [2]

Q.4(b) Differentiate among Information (I), Supervisory(S) and Unnumbered (U) frames used in HDLC protocol. Justify the requirement of S and U frames. [4]

Q.4(c) A sliding window protocol scheme adopts a 3-bit sequence number. At one stage, the transmitter sends frames 0,1,2,3 and 4 and receives acknowledgements for all the sent frames. The station further sends frames 5, 6 and 7 which are also acknowledged. Then the transmitter sends frames 0, 1 and 2. The receiver detects an error in frame 1 and sends NAK 1, which is lost on the way. List out the sequence number of the frames which can be transmitted before the transmitter receives any further ACKs or NAKs, in the following cases due to this error. [6]

i) In Go-back to N ARQ, the transmitter times out
ii) In Go-back to N ARQ, the transmitter does not times out
iii) In Selective Reject ARQ, the transmitter times out
iv) In Selective Reject ARQ, the transmitter does not times out

Q.5(a) What is meant by Subrate multiplexing? Where is it used? [2]

Q.5(b) In an optimized Statistical TDM system, 100 sources each with a data rate of 500bps are to be multiplexed. If the Mean fraction of time each source is transmitting (α) is 0.4, calculate the effective capacity of the multiplexed link (M). Also calculate the Compression (K) and Mean number of items in system (q) per source. [4]

Q.5(c) The following 16 sources are to be multiplexed to obtain a synchronous TDM scheme with a data rate of 360 Kbps: [6]

- Source 1 - Analogue 2.5 KHz bandwidth.
- Source 2 - Analogue 7.5 KHz bandwidth.
- Source 3 - Analogue 10 KHz bandwidth.
- Sources 4 to 8 - Digital sources of 9600 bps synchronous.
- Sources 9 to 14- Digital sources of 3600 bps synchronous.
- Sources 15 to 16 - Digital sources of 19200 bps synchronous.

Implement the scheme as a block diagram, showing all relevant details.

Q.6(a) What is the main disadvantage of Time Slot Interchange (TSI) switch? How is it overcome by using Time Multiplexed Switching (TMS) schemes? [2]

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Q.6(b) In a TS switch No. A - B indicates B^{th} channel in A^{th} TSI stage. If the following connections are required, are connections prone to blocking? If so, which are they? In which time slot? (If two connections are blocking, mention that both are blocking). Which connections are non-blocking? [4]

3 - 6 is to be connected to 1 - 5
2 - 6 is to be connected to 1 - 4
2 - 7 is to be connected to 2 - 4
4 - 7 is to be connected to 4 - 5

Q.6(c) There are 162 stations to be connected through a circuit switch. What will be the number of cross-points required, if a single stage crossbar matrix is adopted? Compare it with the number of cross points required for a 3-stage non-blocking (optimized) switch. How many intermediate stages are required? What is the advantage of second switch over the first switch? [6]

Q.7(a) What is meant by Reassembly Deadlock? How is it avoided in ARPANET network? [2]

Q.7(b) The current routing table for Node 6 in ARPANET original version is given in Table 1. The delay vectors received at Node 6 from the neighboring nodes are given in Table 2. Update Node 6's Routing table based on the delay vectors received. [4]

Destination	Delay	Next Node
1	6	8
2	4	8
3	5	8
4	3	8
5	4	7
6	0	-
7	3	7
8	2	8

Table-1: Node 6's Current directory.

From Node '8'	From Node '7'	From Node '5'	From Node '3'
4	5	6	1
2	2	4	4
3	5	6	0
1	1	2	4
3	1	0	6
2	3	4	5
2	0	1	5
0	2	3	3

Table -2: Delay vectors received at Node 6.

Q.7(c) Find out the least cost path using Dijkstra's algorithm for the network shown in Figure 1. Consider Node 4 as the source node and form Node 4's Routing directory. [6]

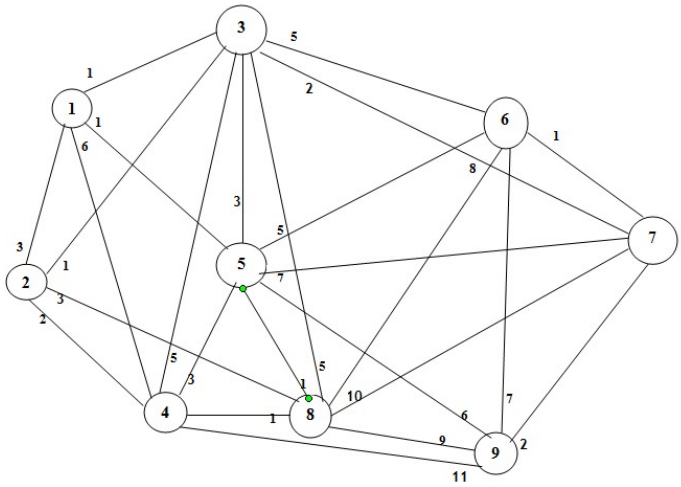

Fig. 1