BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE **SEMESTER: V**
BRANCH: CSE **SESSION : MO/2018**

SUBJECT : EC4205 MICROPROCESSORS AND MICROCONTROLLERS

TIME: 1.5 HOURS **FULL MARKS: 25**

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) What is the difference between macroinstructions and microinstructions? How these instructions are generated by computers? [2]

(b) How Fetch execution overlap is achieved in 8085? Explain by giving suitable timing diagram. [3]

Q2 (a) Which are the status signals available in 8085? What are their functions? [2]

(b) Six unpacked BCD numbers are given at random in 0C20H. Write a program to form the largest 6-digit number which can be formed by them and keep it in 0C40H. [3]

Q3 (a) How a given BCD count in a register is decremented / incremented while programming 8085. [2]

(b) Write a program to choose only BCD numbers from a group of 12 bytes residing in locations starting from 0C20H and add them. Store the sum in BCD in location starting 0C41H. [3]

Q4 (a) What is meant by folded memory? How it could be avoided in a reliable microprocessor system? [2]

(b) How do you interface 2K RAM with 8085, with starting address 4000 H? [3]

Q5 (a) What is the advantage of Interrupt driven I/O operation over the Status check I/O. [2]

(b) 100 bytes are residing in memory location starting from 2400H. Write a 8085 based program to output them serially at SOD pin LSB first MSB last at regular interval of 20msec [3]

Q6 (a) Why interrupt acknowledge signal is generated by 8085 in the following cases [2]
   i) 8085 is interrupted using vectored interrupts pins like RST 5.5 RST 6.5 RST 7.5.
   ii) 8085 is interrupted using non-vectored interrupt pin INTR

(b) Using RST 7.5 interrupt, 16 bytes (maximum value of each data can be only 0CH) are to be inputted through port no. 21H. Write an ISR to input each byte, multiply by 8, convert it to BCD, again multiply it by 10 and store them in locations starting from MULTIDATA. Ensure the interrupts are disabled after receiving 16 bytes. [3]

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