BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: MCA **SEMESTER : I**
BRANCH: MCA **SESSION : MO/18**

SUBJECT: CA403-COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 03:00 **FULL MARKS: 50**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Before attempting the question paper, be sure that you have got the correct question paper.**
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Simplify the given Boolean expression using Boolean algebra properties- [5]
i) $A \oplus AB' \oplus A'$ ii) V+V'W+V'W'X+V'W'X'Y+V'W'X'Y'Z
and also explain De-Morgan's Theorem.

(b) Realize 16:1 MUX using [5]
i) 8:1 MUX
ii) 4:1 MUX

Q.2(a) Explain the functionality of a computer and difference between Byte addressable and word addressable memory. [5]

(b) Consider a hypothetical processor which uses different operand accessing mode shown in below- [5]

Operand Accessing Mode	**Frequency (%)**
1.Register	30
2.Immediate	20
3.Direct	22
4.Memory Indirect	17
5.Indexed	11

Assume that 2 clock cycles consumed for memory reference, 1 clock cycle consumed for arithmetic computation, and 0 clock cycle consumed when operand is in register or instruction itself. What is the average operand fetch rate of the machine?

Q.3(a) What are the differences between hardwired and micro programmed control units? Also explain RISC processor. [5]

(b) Explain different types of hazards that occur in a pipeline. [5]

Q.4(a) In a 2-level memory organization, Level1 memory is 5 times faster than Level2 memory and its access time is 10ns less than average access time. Let Level1 access time is 20ns. What is the hit ratio? [5]

(b) Explain memory hierarchy design. Also explain Set Associative Mapping technique of cache memory. [5]

Q.5(a) Explain Flynn's Classification. [5]

(b) Write a Micro-Program for Fetch Cycle. Explain Types of interrupts. [5]

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